Coater / Developer System Latest Technology

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Hiromitsu Maejima
Clean Track Marketing
Tokyo Electron Limited
Outline

1. EUV technology improvement work
   • In film particle reduction
   • CDU improvement
   • Pattern collapse reduction

2. Coater/Developer system latest technology
   • Rapid detection
   • Autonomous control

3. Summary
EUV technology improvement work
EUV patterning performance improvement using equipment set
CLEAN TRACK™ LITHIUS Pro™ Z
Coater/Developer

Features
- Low particle wafer transfer system
- Improved Overall Equipment Efficiency (OEE) for litho cells
- Reduced Cost of Consumables (CoC) and energy usage

Applications
- EUV, immersion, ArF, KrF, i-line
- 200mm and 300mm wafers

Contact area comparison (after 500 transfers)

Before condition
After LITHIUS Pro™ Z
After conventional

Improved CDU control

Conventional → New
Importance of in-film particle reduction

In-film particle reduction is key to improve defect density

Defect count increases from ADI to AEI

- Thinner pre wet
- Resist dispense
- Resist dry
- Edge/Back Rinse
- Spin dry

In-film particle decrease is key to improve defect density.
EUV defect budget analysis: 24 nm HP CH

After development inspection (ADI)

**ADI Defect Budget**

- Residue defect: 55%
- In-film particle: 44%
- Others: 1%

After etch inspection (AEI)

**AEI Defect Budget**

- Residue defect: 46%
- In-film particle: 52%
- Others: 2%

Residue defect and in-film particle are the dominant before and after etching.
In-film particle reduction measure

**Test Condition**
- Pattern: 45nm LS 1:1
- Filter: HDPE 2nm for Si-ARC
- Track: LITHIUS Pro™ Z
- **Pump for Si-ARC**: Conventional, New dispense system (NDS)
- Metric: Wet particle & AEI TEST Scheme

**Si-ARC wet particle**

![Graph showing the comparison between conventional and NDS systems for wet particle reduction.]

- NDS shows better performance for wet particles/AEI defects than conventional pump.

**AEI Bridge type defect**

![Graph showing the comparison between conventional and NDS systems for AEI Bridge type defects.]

- NDS shows better performance for wet particles/AEI defects than conventional pump.
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Residue defect printability to AEI

- EUV Thru-Etch Defectivity on 24nm Contacts

Residue defect is likely printed 100% through ADI to AEI → Need control
Importance of defect control in developer

DIW pre wet

DEV pre wet

DEV spreading

Rinse

Spin dry

EUV Stochastic Failure Behavior

Bridge

Safe

Collapse/Pinching

Narrow Margin

Large

Line CD

Small

Within Wafer CD Uniformity

Good → Ideal

Bad

Large

Line CD

Small

Residual Droplet Impact

Water droplet

18nm LS Pattern Collapse
Experimental conditions

- Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z-EUV
- EUV Scanner: ASML NXE:3300
- Etching tool: Tactras™
- Inspection tools:
  - Defectivity measurement: KLA2935 from KLA-Tencor
  - Defect review: SEMVision G6 from Applied Materials
  - CD measurement: CG6300 from Hitachi High Technologies
- Materials and Film Layer

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<td>SOC (75nm)</td>
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<td>Si-Ox (20nm)</td>
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<td>Si-Ox (20nm)</td>
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Components and probable contributors for CDU

Coater/developer as well as scanner, mask, and material are probable contributors to CD variation.

For Field to field and Within field CDU improvement, developer process was optimized and compared with conventional condition.

Field to Field and Within field CDU improvement

- Field to field CDU on contact hole 24 nm HP
  - Conventional: 3sigma=0.467
  - Latest measure: 3sigma=0.402
  - 14% improvement

- Within field CDU on contact hole 24 nm HP
  - Conventional: 3sigma=0.892
  - Latest measure: 3sigma=0.835
  - 6.4% improvement

- Latest measure improves both field to field and within field CDU significantly
Wafer to Wafer CDU improvement

Wafer to wafer CD uniformity with batch processing: P = 0.044

3Sigma = 0.281 nm  3Sigma = 0.178 nm

Wafer to wafer CD variation has been improved by 36 % by track process optimization.
How to control pattern collapse

**Capillary force**

\[ \sigma > \frac{6 \gamma \cos \theta}{D} \left( \frac{H}{W} \right) \]

- \( \sigma \): The maximum stress which works to pattern collapse
- \( \gamma \): Surface tension of rinse
- \( \theta \): Contact angle
- \( H \): Height of pattern
- \( D \): Pitch of pattern
- \( W \): Width of pattern
- \( H/W \): Aspect ratio

**Focal point (1)** Low surface tension

![Chart showing surface tension comparison between DIW and FIRM](chart)

**Focus on critical stress (\( \gamma \cos \theta \)) reduction**

**Water droplet**

- Higher contact angle leads to many droplets generation during rinse process.
- \( \rightarrow \) Need contact angle optimization

**Focal point (2)** Surface contact angle optimization

![Diagram showing pattern collapse and hydrophobic surface](diagram)
Optimized rinse performance

- **Contact angle optimization result**
  - Static contact angle (deg)
  - DIW
  - FIRM
  - Latest measure
  - Smooth

- **Minimum CD with no collapse**
  - Improved 3nm
  - DIW: 19.7
  - FIRM: 16.7
  - Latest measure: 13.8
  - Good

- **CD without pattern collapse**
  - Dose
  - DIW
  - FIRM
  - Latest measure
  - Good
  - Collapse
Process window and resist pattern height

- **Process Window**

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- **Pattern height (X-SEM inspection)**

Wider process margin is obtained by latest measure. And pattern height is comparable with existing FIRM process. → Latest measure has a potential which can use more higher aspect ratio of EUV PR pattern.
By applying latest measure to the current process, defect level is drastically improved due to pattern collapse mitigation.
Short summary

TEL optimized coater and developer process.

1. CH Defectivity performance was improved by in-film particle reduction.

2. LS Defectivity margin was extended by pattern collapse reduction.

3. CD uniformity was improved by development process optimization.

TEL continue to improve EUV process for further EUV high-volume manufacturing.
Coater/Developer system future demand
Data use case in semiconductor manufacturing

**Yield**

- Development
- Ramp up
- Mass production

**Challenge**

1. Development time reduction
2. Ramp up time reduction
3. Achieve high Yield and good productivity
4. Automation, Autonomous control which support rapidly expanding Semiconductor manufacturing

**Data use case example**

- Process simulation
- Module and tool matching, automation.
- Smart sampling, monitor, analysis, diagnostic, prediction, correction.

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Data generation and usage is key for semiconductor manufacturing
Rapid detection with integrated wafer inspection

- Deposition
- Lithography (Track-Scanner)
- Etching
- Cleaning
- CMP

Coater → Exposure → Developer → Etching

Compare

Defects:
- Defocus
- Coating Defects (Large Level)
- Coating Defects (Middle Level)
- Baking Defects
- Converge

WIS: Wafer Intelligent Scanner

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Semiconductor manufacturing process steps are huge

Process excursion can cause huge loss. Well balanced Inspection cost, no impact to turn around time are very important.
Semiconductor manufacturing wafer paths are so complicated

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Inspection everywhere

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Macro inspection system with 100% sampling of production wafers
Fast, High and Stable

Customer timeline

Development | Ramp up | HVM (high volume manufacturing)

Matching Analysis

Availability, Performance, Quality

faster

higher

keep

quick recovery

TELeMetrics

WIS

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Summary
Summary

- EUV patterning challenges and TEL’s solutions were reviewed.
- CLEAN TRACK™ LITHIUS Pro™ Z reduces in-film particle, pattern collapse and pattern defect with newly introduced technologies.

- Future demand of coater/developer system is Data generation and usage to minimize the Turn around time (TAT) and process excursion.
- TEL offers valuable contents by using combined Sensor, Tool knowledge, Data analysis technology.
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