ML Platform And Applications

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Challenges in Physical Verification & Semi-Manufacturing Persist at Sub-7nm Technologies

• More Masks
• Larger Dies
• More Simulations
• More Geometrical Processing
• More OPC Layers
• Increasing DRC Operations

• New Resist Materials
• 3D Mask, Resist and Wafer Effects
• New Lithography Techniques – EUV

• Mask Defects
• Lower Process Margins
• Difficult to Detect Yield Limiters

• Higher Design Complexity
• Higher Lithography Development Complexity
• Limited Engineering Resources

Computing Capacity & Turn Around Time
New Process Effects
Reliability & Yield
Productivity
Calibre is the Verification Standard
.......so we see it all!
Calibre **The Bridge Between Design and Silicon**
New Opportunities Enabled by Machine Learning

Finding trends in large sets of unlabeled Data

- Leverages large data volumes
- Useful when less domain knowledge is available

Making predictions based on Trained Data

- Leverages small data volumes & some domain knowledge

Machine Learning in Calibre utilizes both techniques

Reference: Gigaom
Why Machine Learning?

- Relations getting too complicated to identify easily
- Requires quick response (Almost no human interaction)
- Computationally expensive approaches – needs faster sol.

### Supervised Learning

- Classification
- Regression
- Hotspot
- OPC
- Yield Learning from layout
- Yield Retractors using Fab data

### Unsupervised Learning

- Clustering
- Transformation

### Rule Learning

- SRAF
- Retarget
Calibre Architecture Expanded to Integrate Machine Learning Infrastructure

Calibre Machine Learning System

Calibre Core Engine

Calibre Tools & Applications

- Training Data Preparation
- Machine Learning Engine & Model Creation
- Machine Learning Application Programming Interfaces
Calibre ML Platform Overview

- Integrates test pattern generation for ML, model building and model execution seamlessly under one umbrella
- Integrated with full power of SVRF and Calibre (can mix and match use of SVRF and ML functionality)
- Scalable and hierarchical processing capabilities
- Fully programmable by the user for IP protection (C and python interfaces are available)
- Total effort of 20+ men years
Broad Development of Machine Learning Applications in Calibre

IC Fabless
- Physical Design (custom/P&R)
- Physical Verification (DRC/DFM)

IC Foundry
- Mask synthesis (Retarget/RET/OPC)
- Lithography and Etch verification
- Process Step
- Metrology/Inspection
- Electrical test and Failure diagnosis
- Physical failure analysis

Process Step
- Metrology/Inspection

Electrical test and Failure diagnosis
- Physical failure analysis

Lithography Modeling
- Model Accuracy
- Standard Machine Learning

Yield Limiters Detection in Manufacturing

Yield Limiters Detection in Design - LFD

Calibre Machine Learning
ACCURATE MODELING WITH MACHINE LEARNING
## Comparison Image Cognition and OPC model

<table>
<thead>
<tr>
<th></th>
<th>cognitive ability</th>
<th>OPC model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data available</td>
<td># of data: almost no limit</td>
<td># of data: limited, $10^2 \sim 10^4$</td>
</tr>
<tr>
<td>Model/Data update</td>
<td>Relatively easy</td>
<td>difficult</td>
</tr>
<tr>
<td>Feature Vector</td>
<td>16 (CNN by LeCun)</td>
<td>$\sim 100$ (Mentor SONR™)</td>
</tr>
<tr>
<td>Domain</td>
<td>Image itself</td>
<td>Influenced by other process as well as patterning (etch, CMP, thin film,,,)</td>
</tr>
<tr>
<td>Fail Rate</td>
<td>Good if better than human vision error of 6 %</td>
<td>Good only if there is “no” pattern failure $\sim 1e^{-9} \sim 12$</td>
</tr>
</tbody>
</table>

[S. Chennupati, thesis Univ. of Michigan-Dearborn (2016)]

**CNN called LeNet by Yann LeCun (1998)**
Predictability of Machine Learning (ML)

- **Overfit** of flexible (or empirical) model. ML in particular
  - In general, more rigid model shows less overfit while training error smaller.
  - According to Ockham’s razor, more rigid model with smaller parameters preferred.
  - Many parameters should be fitted in ML: A contradiction to principle of Parsimony and a concern of overfit.

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**Ockham’s razor**, William of Ockham (1285~1347)

*FRUSTRA FIT PER PLURA QUOD POTEST FIERI PER PAUCIORA*

Plurality is never to be posited without necessity
System Architecture of Litho Simulation with Neural Network

\[ R(x, y) = \sum_{i=1}^{M} c_i O_i(I(x, y)) \]

A Neural Network is used with inputs being the individual terms of a calibrated resist model

\[ S(x, y) = T \]

\[ S(x, y) = NN(O_i(x, y)), \text{ for all } i \]

Mask (input)

Optical model

\[ I(x, y) \]

Resist model (deconstructed)

\[ O(x, y) \]

NN

Contour

Resist contour (output)

Better architectural choices for using machine learning for modeling in computational lithography are ones that preserve information channels which directly capture physical phenomena:

- Avoid complete black-box modeling
- Maintain manageable requirements for data volume on which to train the models
- Have higher confidence that the final model can extrapolate outside of its training set
- Neural network component is simpler and is responsible for learning only “residual” behaviors

Motto: Do not substitute real intelligence with artificial intelligence
Results

- Convolutional neural network architectures with few hidden layers and careful selection of learnable filters result in good overall solutions for NNAM.
- Sample image and cutline outputs from NNAM:
- Sample CD error plots:
Measuring and Controlling Contour Quality

- The output of simulation in Computational Lithography are contours of the expected printing positions of arbitrary 2D layouts
- Resist (or after-etch) contour data are not always available for the model calibration stage
  — Even when they are available, data size and data quality may be deficient
- A non-disruptive solution must fit in with existing practice
  — Primarily CD-SEM data of high quality is available
- So, how to control “quality” of contours of model output?
- First, we need to measure contour quality

A Neural Network model that learns only from CD data is prone to bad contour predictions – unless provisions are taken

Good (physical) contour
Bad (non-physical) contour

CD_{NNAM}
CD_{CM1}
Accurate & fast etch model required

- Rigorous etch model is NOT available w.r.t. speed, in particular.
- Compact Variable Etch Bias (VEB) model can approximate etch process such as aperture and microloading effects.
- So far VEB model has been successful, but accuracy needs to be improved below 10nm node.
- Many factors in etch process such as ion/radical reaction, chamber geometry power, etc. are not clearly understood

→ a good challenge for Machine Learning
Both accuracy & predictability are improved with ML
— Test case: 10 nm Mx etch, ArFi

\[
\text{Total } 563_{\text{samples}} = 337_{\text{training}} + 113_{\text{validation}} + 113_{\text{test}}
\]

— We improved both accuracy and predictability using ML (about 2 to 4X)

- Accuracy: \( \text{rms}_{\text{training+validation}} \) \( \rightarrow 2.40 \rightarrow 0.65 \text{ nm} \)
- Predictability: \( \text{rms}_{\text{test}} \) \( \rightarrow 2.62 \rightarrow 1.34 \text{ nm} \)
MACHINE LEARNING IN OPC
Higher Computational Demand for IC Design Tapeouts in Sub-7nm Technologies

Predicted Compute Capacity to maintain OPC TAT

Y-axis represents the normalized increase in # of CPU cores to obtain the same OPC TAT. Critical Layer OPC for 100mm^2 chip design using EUV and Multiple Patterning

Increasing computational demand drives the need to continue to speed up OPC
Using Machine Learning in OPC

Data Generation for Training (Uses current OPC model)

Machine Learning Model for OPC

Full Chip OPC (One Machine Learning iteration + two traditional iterations)
3X Runtime Reduction with Calibre Machine Learning OPC

7nm product layer, printed with EUV.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Cumulative OPC CPU Time (hrs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>19806.41</td>
</tr>
<tr>
<td>Machine Learning OPC</td>
<td>5676.97</td>
</tr>
</tbody>
</table>

Reduces computational demand by 3X with improved accuracy

Edge Placement Error (OPC Accuracy Metric): Narrower is Better
Significant Reduction in Computational Demand with Machine Learning OPC in IC Design Tapeouts

Predicted Compute Capacity to Maintain OPC TAT

Y-axis represents the normalized increase in # of CPU cores to obtain the same OPC TAT. Critical Layer OPC for 100mm^2 chip design using EUV and Multiple Patterning
Model based SRAFs
SRAFs placed automatically by model-driven objective function.

Advantages: Simple recipe setup, maximum SRAF coverage of complex 2D geometries. Only ~25% slower than Rulesbased.

Application: Any complex 2D Logic Layouts (Cont/Via/Metals).

Rules based SRAFs
SRAF placement is tuned to ILT mask shapes.

Advantages: Perfectly consistent and deterministic placement.

Application: Ideal for memory arrays, or any situation where perfect consistency is required.

Both solutions can be combined into a “hybrid” recipe.

The industry trend is to use Rules based SRAFs
Model Assisted Template Extractor (MATE)

- MATE was targeted to accelerate the initial SRAF recipe generation, successfully reduced the recipe time from 5 days to 1 day.

- Detailed MATE flow is shown below:

  - **Model-based Solution Generation for Layout Library**
    - Layout library building
    - pxOPC solution generation

  - **Rule Extraction**
    - Rules extraction for number of SRAF
    - Rules extraction for SRAF width and offset

  - **Recipe Generation**
    - Edge classification
    - cnSRAF recipe generation
MATE: Machine Learning For SRAF Insertion

- Rules-based SRAF insertion is faster and more consistent than Model-based.
- Accuracy is often lower, due to the complexity of the placement rules.
- We have applied Decision Tree Learning to enable RB-SRAF rule generation, providing accuracy similar to Inverse Lithography ‘golden standard’.

Run pxOPC (ILT) to generate ‘golden’ SRAFs.

Analyze golden SRAFs with Decision Tree Learning system.

Output fully functional RB SRAF recipe.

Matching RB-SRAFs
MATE Results

- Example result for 7nm Cut Layer.
HOTSPOT DETECTION AND ANALYSIS WITH MACHINE LEARNING
LFD Detects Yield Limiters Prior to Manufacturing at Design Stage

https://www.techdesignforums.com/practice/technique/quantifying-returns-on-litho-friendly-design/
LFD with Machine Learning – Faster Path to Results

Machine Learning: Identify Areas of Interest
- Improve Coverage
- Reduce Unnecessary Simulation Area
- Improve Runtime Performance

Lithography Simulation
- Yield Limiters Detection

Design Layout

Areas of Interest For Simulation

Yield Limiters & Design Fixing Guidelines
Using Machine Learning in LFD

Data Generation for Training
(Can include broad range of systematic processing defects)

Machine Learning Model for LFD

Output with Predicted Yield Limiters & Design Fixing Guidelines
LFD with Machine provides Significant Speedup while Finding New Yield Limiters

- 10X Speedup in LFD Time
- Yield Limiters in Training Set
- Previously Undetected Yield Limiters

Calibre Machine Learning System
What is SONR? – Un/Semi supervised learning

- Calibre **SONR** is a new product combining multiple related applications under one license.

- SONR uses feature vectors which are shown to correlate well with fab printing behavior. Layout shapes with similar feature vectors are shown to behave similarly in the fab.

- **SONR Layout Analysis**
  - Uses unsupervised Machine Learning methods to enable layout reduction and comparison.
    - Reduce a layout to minimum set of representative patterns.
    - Compare 2 layouts to find unique patterns.

- **SONR Hotspot Prediction** (semi-supervised)
  - Given knowledge of existing hotspot locations, predict new hotspots.

- **SONR Hotspot Prediction** (Supervised)
  - Given knowledge of existing hotspot locations, build a model to predict new hotspots.
SONR ML Hotspot Prediction (Supervised)

- Trained Machine Learning model predicts new hotspot.
SONR ML Hotspot Prediction (Supervised)

- Trained Machine Learning model predicts new hotspot.

![Diagram](image)

**Input**
- Layout A
- Known Hotspot Coordinates
- Trained Hotspot Model
- Litho Models
- Feature Vector 1
- Feature Vector 2

**Output**
- SONR predicted Hotspots
- Not Hotspots

**Database**
- New Hotspots
CONCLUSIONS
In Conclusion

- Calibre is the bridge between Design to Silicon – complete solution that covers the entire Tapeout flow

- Leveraging Machine Learning on the Calibre platform to provide faster, smarter and more accurate solutions to meet the design and manufacturing needs of today and the future